EXHIBIT B

Page 1 of the document is a letter dated July 8, 2002.

This is its English translation:

"Our ref.: ***02-AG-029/RR*** *Agrate, 8 July 2002*

Subject: Filing of a patent application in the name of
STMicroelectronics S.r.l.

Inventor:

PIVIDORI Luca

We ask you to file, by using the annexed document, an European patent application for an invention related to:

PROTECTION OF A PRE-METAL LAYER FOR DEFINING CONTACTS LESS THAN 0.21um IN NON VOLATILE MEMORY DEVICES.

It would be desirable that the application is filed within

31 August 2002

because there is a possibility of disclosure of the invention.

The States to designate in the application are Italy, France, Great Britain, Germany and the language to use is the English.

For further technical information please contact the inventors, at the laboratories.

With the occasion, we give you our best greetings.

STMicroelectronics S.r.l.

copy to: inventors

The second page of the document is already in English except for the descriptive title of the invention which is:

PROTECTION OF A PRE-METAL LAYER FOR DEFINING CONTACTS LESS THAN 0.21um IN NON VOLATILE MEMORY DEVICES.

This page comprises the name and the address of the inventor.

Pividori Luca
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The translation in English of the document from the third page to the sixth page is:

Agrate, January 10, 2002

From: Luca Pividori *to: Patent Office Agrate*

-Patent proposal-

PROTECTION OF A PRE-METAL LAYER FOR DEFINING CONTACTS LESS THAN 0.21um IN NON VOLATILE MEMORY DEVICES.

Problem description:

The idea that constitutes this patent allows to solve two drawbacks which occur in the process for defining contacts in 0.15um or lower processes (however this idea can be implemented in less critical technologies)

The method which is herein described results simpler and it is easy to locate by means of an analysis with the SEM section in any region of the wafer because the contacts are formed everywhere both in the matrix regions and in the circuit regions.

State of the art:

The state of the art typically comprises all the steps of process which are used by the authorized personnel to form the structures necessary to define the matrix regions or the circuit regions of a flash memory device.

Once the active areas of the circuitry and of the matrix memory of the flash device are formed the process steps are effected which represent the state of the art to produce these devices:

1) Growth of an active oxide (tunnel);

2) Deposition and definition of a polysilicon layer that constitutes the floating gate (poly1) only in the active matrix and its elimination from the circuits;

3) Deposition of a dielectric interpoly layer (typically ONO);

4) Through a mask, said MATRIX mask, the attack (generally in dry) of the deposed layers of oxide interpoly (typically ONO) and of the polysilicon of the floating gate memory cells it is effected;

5) Growth of one or more layers of gate active oxides;

6) Deposition of a second layer of polysilicon;

7) Definition of the matrix cells through exposure of the auto-alignment mask;

8) Definition of the transistors gates through exposure of the circuit mask.

Subsequently the formation of the layer in which should be generated the contacts is effected.

9) Deposition of an oxide layer typically from HDP process with a thickness among 500Å-2500Å, or of nitride (in the case in which for the formation of said contacts a process called borderless is used),

10) Deposition of a layer of BPSG, generally through a SACVD process, with concentration of the type 2:9 useful especially for memory flash devices.

11) Thermal treatment with RTA of the deposed BPSG layer.

12) Planarization of the pre-metal layer (USG+BPSG) for instance through CMP technology.

At this point, according to the known art the contact mask is exposed, which foresees the deposition from the lithographic machine of two overlapped layers of BARC and of resist, for the masks of the DUV type. Such layers are necessary to allow the correct definition of the contacts according to the dimensional specifications required by the product, by preventing even the contamination of the resist DUV from the doped layer of BPSG.

Proposed process:

The idea that constitutes the invention of this patent is that of proceeds in the following way:

After the phase 12), instead of immediately exposing the contact mask, a transparent UV nitride layer is deposed through a HDP process, with a thickness from 200Å to 500Å (indicated by the reference 5 in the drawings relative to the process).

The function of this layer is:

a) avoiding the direct contact of the BARC+resist with the BPSG, also in case of prolonged rest of the wafers with BARC+resist already deposed and before their working. In such a way the defectiveness formation called "corrosion" of the BPSG layer is avoided, which makes impossible the contact definition and therefore provokes a yield loss during the device testing (Fig. 1).

b) avoiding the formation of contacts called "with double edge", as disclosed in Fig. 2, that are critical when the contact dimension is of the order of the 0.2 um or smaller than that and the distance between the contacts is of the order of 0.5um.

The deposed layer must be of a material that allows of getting a high selectivity with the BPSG during the contact attack, so that, once the resist is worn out (or it has been consumed) it develops the same function of upper barrier layer (that is above the BPSG layer) in comparison to the attack chemistry. To this purpose it could be advantageous that the deposed layer is for instance a transparent UV nitride that has high selectivity with the BPSG and does not prevent the reliability performances of the memory cell, particularly if the cell is of flash type.

Once the barrier layer has been deposed according to the patent proposal, the normal operations of mask exposure of the contact and its attack is effectuated (indicated by the reference 6 in the drawings relative to the process). Obviously the contact attack chemistry will be modified in order to correctly attach the additional protective layer in the first steps by proceeding in a standard way with the chemistry of the oxide etch once it is arrived on the BPSG.

The use of such a technology is immediately identifiable because the protective layer must be left on the surface of the BPSG.